

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1, 3, 6-9 and 12 have been amended. Claim 4 has been canceled without prejudice. New claims 15-21 have been added.

1. (Currently Amended) A method for scheduling access to a device comprising:
tracking a current state of a device;
tracking a count of a number of requests which require a particular state; and
scheduling requests to the device using the current state of the device, the count of the number of requests that have already been scheduled using the current state, a threshold value established for a switch point indicating when to switch state, wherein after the count reaches the switch point and there are incoming requests having an alternate state to the current state of the device, switching the state of the device to process incoming requests.
2. (Original) The method as set forth in claim 1, further comprising configuring the switch point.
3. (Currently Amended) The method as set forth in claim 2, wherein the switch point is dynamically configurable adjustable by software.
4. (Canceled)

5. (Original) The method as set forth in claim 1, wherein the device is a dynamic random access memory (DRAM) a scheduler type is selected from the group consisting of a DRAM bus turnaround scheduling, DRAM page scheduling and DRAM physical bank switching.

6. (Currently Amended) A bus scheduler comprising:
an input configured to receive at least one incoming request, each request indicating a bus direction;
a switch point;
an indicator of a current bus direction;
a unit to track a count of requests processed using the current bus direction; and
logic configured to switch the direction of the bus to process incoming requests wherein after the count reaches a threshold value established for the switch point and there are incoming requests having the direction opposite to the current direction of the device bus, switching the direction of the device bus.

7. (Currently Amended) The bus scheduler as set forth in claim 6, wherein the threshold value established for the switch point is configurable.

8. (Currently Amended) A scheduler comprising:
a switch point;
a first unit to track a current device state of a device;
a second unit to track a count of requests that require a particular state;

logic configured to determine an updated device state using the switch point and count such that when the count crosses a threshold of the switch point, the device state is changed; and

scheduling logic configured to ~~scheduling~~ schedule access requests to the device using the updated device state.

9. (Currently Amended) The scheduler as set forth in claim 8, wherein a value of the threshold established for the switch point is dynamically configurable via software.

10. (Original) The scheduler as set forth in claim 8 wherein the device comprises a bus and the device state comprises a bus direction, said scheduling dependent upon the bus direction.

11. (Original) The scheduler as set forth in claim 8, wherein the device is a dynamic random access memory (DRAM) and scheduling is selected from the group consisting of DRAM bus turnaround scheduling, DRAM page scheduling and DRAM physical bank switching.

12. (Currently Amended) The scheduler as set forth in claim 6, wherein the threshold value established for switch point is software configurable.

13. (Original) The scheduler as set forth in claim 8, wherein the device comprises a DRAM with multiple pages and the device state comprises the identity of at least one open page, said scheduling dependent on the at least one page opened.

14. (Original) The scheduler as set forth in claim 8, wherein the device comprises a DRAM with multiple physical banks and the device state comprises the last accessed physical bank, said scheduling dependent on the last accessed physical bank.

15. (New) The scheduler as set forth in claim 8, further comprising:
a register to store the threshold number of counts to establish the switch point.

16. (New) The bus scheduler as set forth in claim 6, further comprising:
a register to store the threshold number of counts to establish the switch point.

17. (New) The scheduler as set forth in claim 8, wherein the scheduler is embedded on a System on a Chip.

18. (New) The bus scheduler as set forth in claim 6, wherein the bus scheduler is embedded on a System on a Chip.

19. (New) The scheduler as set forth in claim 8, further comprising:
a controller of a volatile memory coupled to the scheduler; and

filter logic configured to combine thread quality of service scheduling and volatile memory scheduling to reorder servicing requests from one or more threads based on achieving a highest usage efficiency of the volatile memory while still satisfying quality of service guarantees for each thread.

20. (New) The bus scheduler as set forth in claim 6, further comprising:

a controller of a volatile memory coupled to the scheduler via the bus; and

filter logic configured to combine thread quality of service scheduling and volatile memory scheduling to reorder servicing requests from one or more threads based on achieving a highest usage efficiency of the volatile memory while still satisfying quality of service guarantees for each thread.

21. (New) An apparatus to scheduling access to a device comprising:

means for tracking a current state of a device;

means for tracking a count of a number of requests which require a particular state; and

means for scheduling requests to the device using the current state of the device, the count of the number of requests that have already been scheduled using the current state, a threshold value established for a switch point indicating when to switch state, wherein after the count reaches the switch point and there are incoming requests having an alternate state to the current state of the device, switching the state of the device to process incoming requests.